



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,305	10/27/2000	Takaki Yoshida	YMOR:186	4222

7590 01/02/2004

PARKHURST & WENDEL, LLP
1421 Prince Street, Suite 210
Alexandria, VA 22314

EXAMINER

TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
----------	--------------

2133

DATE MAILED: 01/02/2004

11

Please find below and/or attached an Office communication concerning this application or proceeding.

3

Office Action Summary

Application No.

09/697,305

Applicant(s)

YOSHIDA ET AL.

Examiner

Joseph D. Torres

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 November 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-52 is/are pending in the application.
- 4a) Of the above claim(s) 23-52 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5, 12-14 and 16 is/are rejected.
- 7) ☒ Claim(s) 4, 6-11, 15 and 17-22 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 October 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Note: Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Election/Restrictions

2. This application contains claims 23-52 drawn to an invention nonelected with traverse in Paper No. 6. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Objections

3. Claims 1-22 are objected to because of the following informalities:

Claim 1 recites the limitation, "corresponding to (a) information identifying locations of a semiconductor integrated circuit where a possible-fault is likely to occur or (b) information required to reduce faults". The Examiner would like to point out that the connector 'or' only requires that one of the limitations be present. Since fault lists generally provide "information required to reduce faults" by providing a mechanism to

analyze circuit design so that circuits can be redesigned to reduce faults or by allowing for replacement of faulty circuitry by redundant parts, it is unclear how the previously quoted limitation in claim 1 further limits claim 1.

Claim 6 should be corrected for grammatical errors.

Claim 12 recites similar language.

Claims 2-11 and 13-22 depend from respective claims 1 and 12, hence inherit the deficiencies in claims 1 and 12.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh).

35 U.S.C. 102(e) rejection of claim 1 and 12.

Rohrbaugh teaches a fault detecting method for a semiconductor integrated circuit (Figure 1 in Rohrbaugh exemplifies a test setup using a Test Generator 102 and

Automatic Test Equipment, ATE 104, in Figure 1 of Rohrbaugh for use in the fault detecting method for a semiconductor integrated circuit described in col. 5, lines 8-21, Rohrbaugh), comprising: providing a fault list (the Fault List in step 702 of Figure 7 of Rohrbaugh is a typical Fault list used by Test Generator 102 in Figure 1 of Rohrbaugh for generating a compacted set of test vectors) corresponding to a. information identifying locations of a semiconductor integrated circuit where a possible-fault is likely to occur (col. 2, lines 15-20 of Rohrbaugh teach that a fault list is a listing of locations where faults may occur) or b. information required to reduce faults (a fault list is information that can be used to reduce faults by providing fault information in the manufacturing or design phase so that corrective actions can be taken, such as; replacing faulty circuitry with redundant circuitry); and detecting faults in a semiconductor integrated circuit to which said fault list corresponds by using said fault list (the Abstract in Rohrbaugh teaches a method for creating a fault list used in the Test Generator 102 and Automatic Test Equipment, ATE 104, in Figure 1 of Rohrbaugh for creating test patterns to detect faults in DUT 116 in Figure 1 of Rohrbaugh; hence Rohrbaugh teaches detecting faults in a semiconductor integrated circuit, DUT 116, to which said fault list corresponds by using said fault list to generate test patterns).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

Art Unit: 2133

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
5. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh) in view of Goel, Prabhakar (US 4204633 A).

35 U.S.C. 103(a) rejection of claims 2 and 13.

Rohrbaugh, substantially teaches the claimed invention described in claims 1 and 12 (as rejected above).

However Rohrbaugh, does not explicitly teach the specific use of "omitting possible faults that are difficult to detect from the fault list".

Goel, in an analogous art, teaches "omitting possible faults that are difficult to detect from the fault list" (col. 2, lines 66-68, Goel teaches that faults which occur at a frequency below a predetermined level are eliminated from the set of faults; Note: faults which occur at a frequency below a predetermined level are faults that are difficult to detect due to the lack of frequency of occurrence). The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have been highly

Art Unit: 2133

motivated to combine the Rohrbaugh patent with the Goel patent since Rohrbaugh teaches automatic test system that requires that a fault list be defined (see Step 702 of Figure 7 in Rohrbaugh) in order to generate test pattern but does not teach the details of how that fault list is generated and Goel teaches the specifics of defining a fault list for a pattern generator used in automatic test equipment (col. 2, lines 42-46, Goel). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Rohrbaugh with the teachings of Goel by including an additional step of "omitting possible faults that are difficult to detect from the fault list". This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that "omitting possible faults that are difficult to detect from the fault list" would have provided the opportunity to speed up testing by eliminating faults with a low probability of occurrence thereby reducing the number of faults needed (col. 2, lines 66-68, Goel).

6. Claims 3, 5, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh) in view of NN9205250 ("Improved Method for Weighted Random Pattern Weight Generation", IBM Technical Disclosure Bulletin, May 1992, US, NN9205250).

35 U.S.C. 103(a) rejection of claims 3, 5, 14 and 16.

Rohrbaugh, substantially teaches the claimed invention described in claim 1 (as rejected above).

However Rohrbaugh, does not explicitly teach the specific use of the fault list comprising likelihood data of a fault.

NN9205250, in an analogous art, teaches a fault list comprises likelihood data of a fault (Note: NN9205250 teaches a Weighted Random Pattern Weight Generator that uses a fault list for pattern generation whereby faults in the fault list are weighted with likelihood information). The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have been highly motivated to combine the Rohrbaugh patent with the NN9205250 since Rohrbaugh teaches automatic test system that requires that a fault list be defined (see Step 702 of Figure 7 in Rohrbaugh) in order to generate test pattern but does not teach the details of how that fault list is generated and NN9205250 teaches the specifics of defining a fault list for a pattern generator used in automatic test equipment (see NN9205250).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Rohrbaugh with the teachings of NN9205250 by including use of the fault list comprising likelihood data of a fault. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the fault list comprising likelihood data of a fault would have provided the opportunity to efficiently generate logic test by minimizing the number of test patterns required (see NN9205250).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

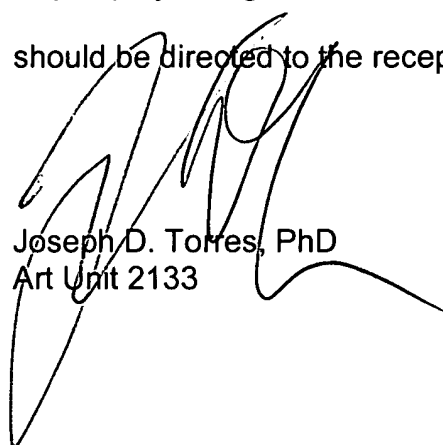
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Art Unit: 2133

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.



Joseph D. Torres, PhD
Art Unit 2133



ALBERT DEADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100